

H

PTO/SB/05 (4/98)

Approved for use through 09/30/2000 OMB 0651-0032

Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

12/30/99

Please type a plus sign (+) inside this box



**UTILITY
PATENT APPLICATION
TRANSMITTAL**

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	042390.P6785
First Inventor or Application Identifier	Nagesh Vodrahalli
Title	HIGH PERFORMANCE THERMAL INTERFACE CURING PROCESS FOR ORGANIC FLIP CHIP PACKAGES
Express Mail Label No.	EL236787001US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

1. <input checked="" type="checkbox"/> Fee Transmittal Form <i>(Submit an original, and a duplicate for fee processing)</i>	5. <input type="checkbox"/> Microfiche Computer Program (Appendix)
2. <input checked="" type="checkbox"/> Specification [Total Pages 12] <i>(preferred arrangement set forth below)</i>	6. Nucleotide and/or Amino Acid Sequence Submission <i>(if applicable, all necessary)</i>
- Descriptive title of the Invention	a. <input type="checkbox"/> Computer Readable Copy
- Cross References to Related Applications	b. <input type="checkbox"/> Paper Copy (identical to computer copy)
- Statement Regarding Fed sponsored R & D	c. <input type="checkbox"/> Statement verifying identity of above copies
- Reference to Microfiche Appendix	
- Background of the Invention	
- Brief Summary of the Invention	
- Brief Description of the Drawings (if filed)	
- Detailed Description	
- Claim(s)	
- Abstract of the Disclosure	
3. <input checked="" type="checkbox"/> Drawing(s) (35 U.S.C. 113) [Total Sheets 2]	
4. Oath or Declaration [Total Pages 3]	
a. <input type="checkbox"/> Newly executed (original copy)	7. <input type="checkbox"/> Assignment Papers (cover sheet & document(s))
b. <input type="checkbox"/> Copy from a prior application (37 C.F.R. § 1.63(d)) <i>(for continuation/divisional with Box 16 completed)</i>	8. <input type="checkbox"/> 37 C.F.R. § 3.73(b) Statement <input type="checkbox"/> Power of Attorney <i>(when there is an assignee)</i>
i. <input type="checkbox"/> DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §§ 1.63(d)(2) and 1.33(b).	9. <input type="checkbox"/> English Translation Document (if applicable)

*NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY
SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED
(37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS
RELIED UPON (37 C.F.R. § 1.28).

ACCOMPANYING APPLICATION PARTS

10. <input type="checkbox"/> Information Disclosure Statement (IDS)/PTO - 1449	<input type="checkbox"/> Copies of IDS Citations
11. <input type="checkbox"/> Preliminary Amendment	
12. <input type="checkbox"/> Return Receipt Postcard (MPEP 503) <i>(Should be specifically itemized)</i>	
13. <input type="checkbox"/> *Small Entity Statement(s)	<input type="checkbox"/> Statement filed in prior application, Status still proper and desired
14. <input type="checkbox"/> Certified Copy of Priority Document(s) <i>(if foreign priority is claimed)</i>	
15. <input type="checkbox"/> Other:

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

Continuation Divisional Continuation-in-part (CIP) of prior application No: _____

Prior application Information: Examiner _____ Group/Art Unit: _____

For CONTINUATION or DIVISIONAL APPS only. The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

<input type="checkbox"/> Customer Number or Bar Code Label	(Insert Customer No. or Attach bar code label here)		or	<input checked="" type="checkbox"/> Correspondence address below
Name	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP			
Address	12400 Wilshire Boulevard, Seventh Floor			
City	Los Angeles	State	California	Zip Code
Country	U.S.A.	Telephone	(714) 557-3800	Fax

Name (Print/Type)	Ben J. Yorks, Reg. No. 33,609
-------------------	-------------------------------

Signature	
-----------	--

Date	12/30/99
------	----------

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

Our File No.: 042390.P6785
Express Mail No.: EL236787001US

UNITED STATES PATENT APPLICATION

FOR

HIGH PERFORMANCE THERMAL INTERFACE CURING PROCESS FOR
ORGANIC FLIP CHIP PACKAGES

INVENTORS: Nagesh Vodrahalli
Biswajit Sur

PREPARED BY:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN
12400 Wilshire Blvd., 7th Floor
Los Angeles, CA 90025-1026
(714) 557-3800

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

5 The present invention relates to a process for curing a thermal epoxy that couples an integrated circuit to a thermal element.

2. BACKGROUND INFORMATION

10 Integrated circuits can be assembled into packages that are soldered to a printed circuit board. The integrated circuit is typically mounted to a substrate and enclosed by an encapsulant. Integrated circuits generate heat that must be removed from the package. Some integrated circuit packages incorporate thermal elements such as heat spreader to improve the thermal performance of the package. The heat spreader may be coupled to a surface of the integrated circuit by a thermal grease or a thermal epoxy.

15 The thermal epoxy may be cured in an oven that heats the entire package. The coefficient of thermal expansion of the substrate is typically different than the expansion coefficient of the integrated circuit and the thermal element. When the thermal epoxy is heated in the oven the different coefficient of expansions may create a warpage in the package. The warpage may induce a pumping

action of the thermal epoxy so that epoxy flows out of the integrated circuit/thermal element interface. This pumping event may create an air gap between the integrated circuit and the thermal element. Air has a low coefficient of thermal conductivity. The existence of air increases the thermal impedance of the package and the junction temperatures of the integrated circuit. It would be desirable to provide a process that cures the thermal epoxy without heating the other elements of the package.

SUMMARY OF THE INVENTION

One embodiment of the present invention is an integrated circuit package which has a thermal epoxy that can be attached to an integrated circuit and a thermal element. The thermal epoxy can be cured with energy at a microwave frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view of an embodiment
of an integrated circuit package of the present
invention;

Figures 2a-b show a process for assembling a thermal
epoxy within the integrated circuit package;

Figures 3a-b show an alternate process for assembling
the thermal epoxy within the package.

DETAILED DESCRIPTION

Referring to the drawings more particularly by reference numbers, Figure 1 shows an embodiment of an integrated circuit package 10 of the present invention. The package 10 may include an integrated circuit 12 that is mounted to a substrate 14. The integrated circuit 12 may be mounted to the substrate 14 with a plurality of solder bumps 16 in a process commonly referred to as controlled collapsed chip connection (C4). The package 10 may further have an underfill material 18 attached to the integrated circuit 12 and the substrate 14 to improve the structural integrity of the solder bumps 16.

The package 10 may have a plurality of solder balls 20 attached to the substrate 14 in a ball grid array (BGA) pattern. The solder balls 20 may be reflowed to attach the package 10 to a printed circuit board (not shown) such as the motherboard of a computer. The substrate 14 may contain routing traces, power/ground planes, vias, etc. that electrically connect the solder bumps 16 to the solder balls 20. Although solder balls 20 are shown and described, it is to be understood that the package 10 may have other types of contacts such as pins.

The package 10 may have a thermal epoxy 22 that is attached to a thermal element 24 and the integrated circuit 12. The thermal element 24 may be a heat

spreader that is constructed from a thermally conductive material such as copper or aluminum. The thermal epoxy 22 may be an epoxy resin that contains a thermally conductive filler such as carbon particles. The thermal 5 epoxy 22 provides a thermal path from the integrated circuit 12 to the thermal element 24. The integrated circuit 12 may be enclosed by an encapsulant 26.

Figures 2a and 2b show a method for constructing the package 10. The integrated circuit 12 is typically 10 mounted to the substrate 14 by the solder bumps 16 and underfill material 18. As shown in Fig. 2a an uncured thermal epoxy 22 is applied to the top surface of the integrated circuit 12. By way of example, the uncured epoxy 22 may be applied with a screening process that 15 utilizes a template (not shown).

As shown in Fig. 2b the thermal element 24 is placed onto the thermal epoxy 22 and the epoxy 22 is cured by a microwave generator 28. The microwave generator 28 generates energy at a microwave frequency that is 20 directed into the thermal epoxy 22. The microwave frequency can be selected to cure the thermal epoxy 22 without damaging the integrated circuit 12 or heating the other components of the package 10. Not heating the other package components eliminates package warpage and 25 epoxy pumping that can create air gaps and voids in the integrated circuit/thermal element interface. By way of example, the microwave energy may have a frequency

between _____ and _____ megahertz. After the thermal epoxy 22 is cured the encapsulant 26 can be formed into the package with an injection mold process. The solder balls 20 can then be attached to the substrate 14 to 5 complete the assembly. It may be desirable to bake the substrate 14 before curing the thermal epoxy 22 to insure that the curing process does not release water from the substrate material.

Figures 3a and 3b show an alternate method for 10 assembling the thermal epoxy 22, wherein the epoxy 22 is applied to the thermal element 24 instead of the integrated circuit 12 before being cured by the microwave generator 28.

While certain exemplary embodiments have been 15 described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and 20 described, since various other modifications may occur to those ordinarily skilled in the art.

CLAIMS

What is claimed is:

1 1. An integrated circuit package, comprising:
2 a substrate;
3 an integrated circuit mounted to said substrate;
4 a thermal element located adjacent to said integrated
5 circuit; and,
6 an epoxy that is attached to said integrated circuit
7 and said thermal element, said epoxy being cured by
8 energy at a microwave frequency.

1 2. The package of claim 1, further comprising a
2 solder ball attached to said substrate.

1 3. The package of claim 1, further comprising a
2 solder bump attached to said integrated circuit and said
3 substrate.

1 4. The package of claim 1, further comprising an
2 encapsulant that encloses said integrated circuit.

1 5. A method for assembling an integrated circuit
2 package, comprising:
3 applying an epoxy to an integrated circuit;
4 placing a thermal element adjacent to the epoxy; and,

5 curing the epoxy with energy at a microwave
6 frequency.

1 6. The method of claim 5, further comprising the
2 step of mounting the integrated circuit to a substrate.

1 7. The method of claim 6, further comprising the
2 step of attaching a solder ball to the substrate.

1 8. The method of claim 5, further comprising the
2 step of molding an encapsulant onto the substrate and the
3 integrated circuit.

1 9. A method for assembling an integrated circuit
2 package, comprising:

3 applying an epoxy to a thermal element;
4 placing the epoxy and the thermal element onto an
5 integrated circuit; and,
6 curing the epoxy with energy at a microwave
7 frequency.

1 10. The method of claim 9, further comprising the
2 step of mounting the integrated circuit to a substrate.

1 11. The method of claim 10, further comprising the
2 step of attaching a solder ball to the substrate.

1 12. The method of claim 9, further comprising the
2 step of molding an encapsulant onto the substrate and the
3 integrated circuit.

ABSTRACT OF THE DISCLOSURE

An integrated circuit package which has a thermal epoxy that can be attached to an integrated circuit and a thermal element. The thermal epoxy can be cured with energy at a microwave frequency. Curing the thermal epoxy with microwave energy can minimize package warpage during the curing process.

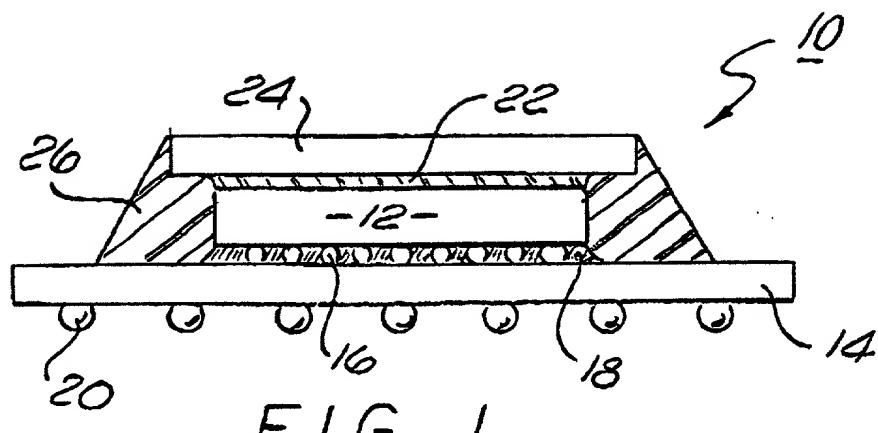


FIG. 1

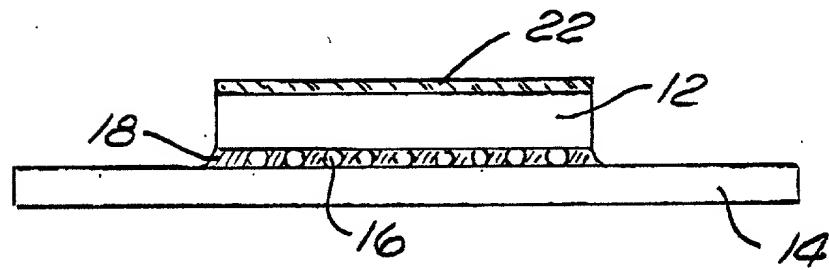


FIG. 2a

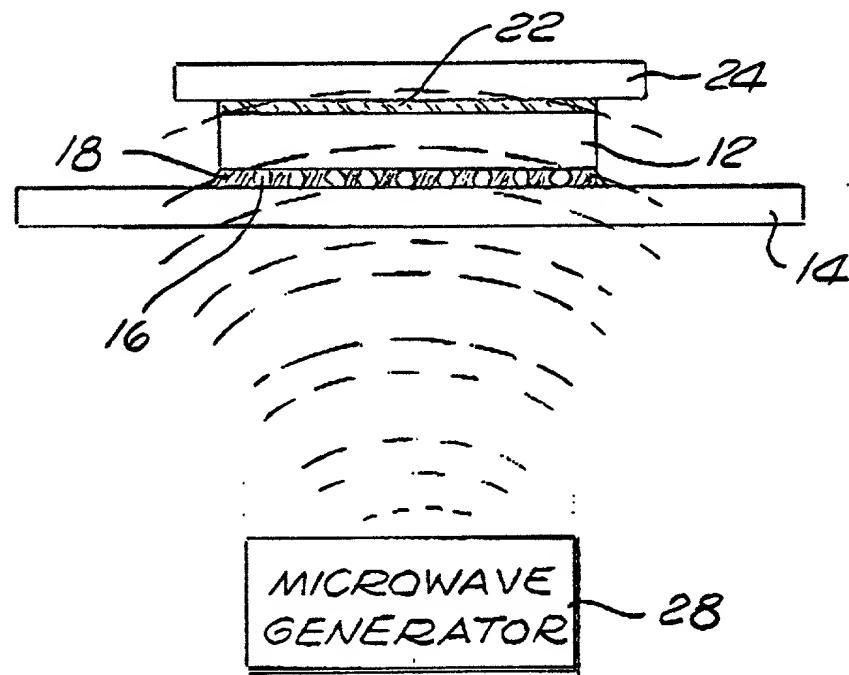


FIG. 2b

**DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR INTEL CORPORATION PATENT APPLICATIONS)**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

**HIGH PERFORMANCE THERMAL INTERFACE CURING PROCESS FOR ORGANIC
FLIP CHIP PACKAGES**

the specification of which



is attached hereto.

was filed on _____ as _____

United States Application Number _____

or PCT International Application Number _____

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 37 USC 119
			<input type="checkbox"/> No <input type="checkbox"/> Yes
			<input type="checkbox"/> No <input type="checkbox"/> Yes
			<input type="checkbox"/> No <input type="checkbox"/> Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, a firm including: William E. Alford, Reg.37,764; Farzad E. Amini, Reg. No. 42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Lawrence M. Cho, Reg. No. 39,942; Yong S. Choi, Reg. No. 43,324; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; Barbara Bokanov Courtney, Reg. No. P42,442; William Donald Davis, Reg. No. 38,428; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Tarek N. Fahmi, Reg. No. P41,402; James Y. Go, Reg. No. 40,621; Richard Leon Gregory, Jr., P42,607; Dinu Gruia, Reg. No. 42,996; David R. Halvorson, Reg. No. 33,395; Thomas A. Hassing, Reg. No. 36,159; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. P41,845; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Tim L. Kitchen, Reg. No. P41,900; Michael J. Mallie, Reg. No. 36,591; Paul A. Mendonsa P42,879; Darren J. Milliken, P42,004; Thinh V. Nguyen, Reg. No. 42,034; Kimberley G. Nobles, Reg. No. 38,255; Michael A. Proksch P43,021; Babak Redjaian, Reg. No. 42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. 43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Geoffrey T. Staniford, P43,151; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, P43,237; Charles T. J. Weigell, Reg. No. 43,398; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Amy M. Armstrong, Reg. No. P42,265; Robert Andrew Diehl, Reg. No. P40,992; and Edwin A. Sloane, Reg. No. 34,728; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (714) 557-3800, and Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Sean Fitzgerald, Reg. No. 32,027; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; and Charles K. Young, Reg. No. 39,435; my patent attorneys, of INTEL CORPORATION with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Ben J. Yorks, Reg. No. 33,609, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)

ZAFMAN LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to Ben J. Yorks, Reg. No. 33,609, (714) 557-3800.

(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor (given name, family name)

Nagesh Vodrahalli

Inventor's Signature _____

Date _____

Residence Cupertino, California USA

Citizenship USA

(City, State)

(Country)

P. O. Address 20276 Pinntage Parkway

Cupertino, California 95014 USA

Full Name of Second/Joint Inventor (given name, family name)

Biswajit Sur

Inventor's Signature _____

Date _____

Residence San Jose, California USA

Citizenship India

(City, State)

(Country)

P. O. Address 6915 Rockton Avenue

San Jose, California 95119 USA

Full Name of Third/Joint Inventor (given name, family name)

Inventor's Signature _____

Date _____

Residence _____

Citizenship _____

(City, State)

(Country)

P. O. Address _____

Full Name of Fourth/Joint Inventor (given name, family name)

Inventor's Signature _____

Date _____

Residence _____

Citizenship _____

(City, State)

(Country)

P. O. Address _____